FIG. 1

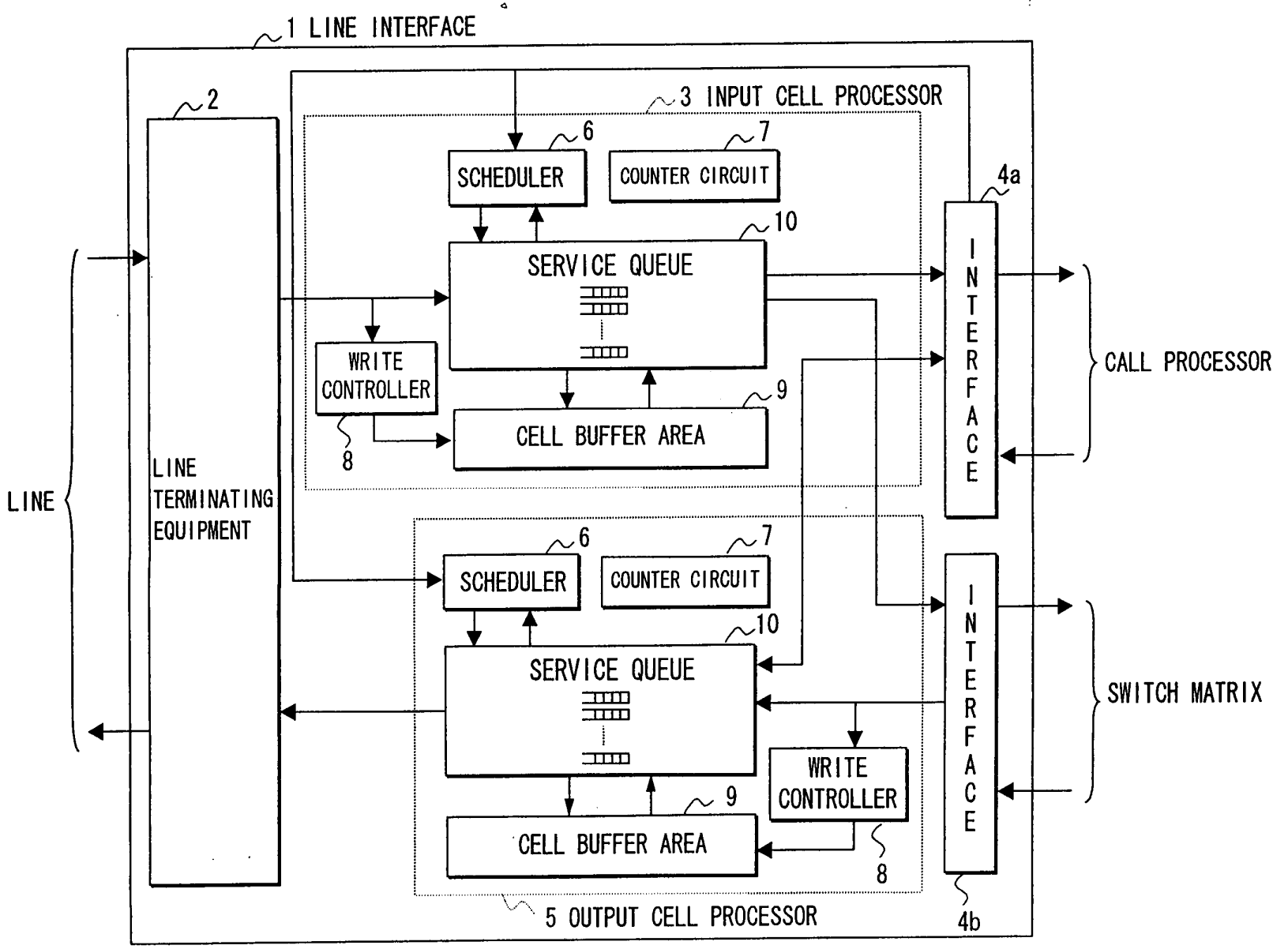
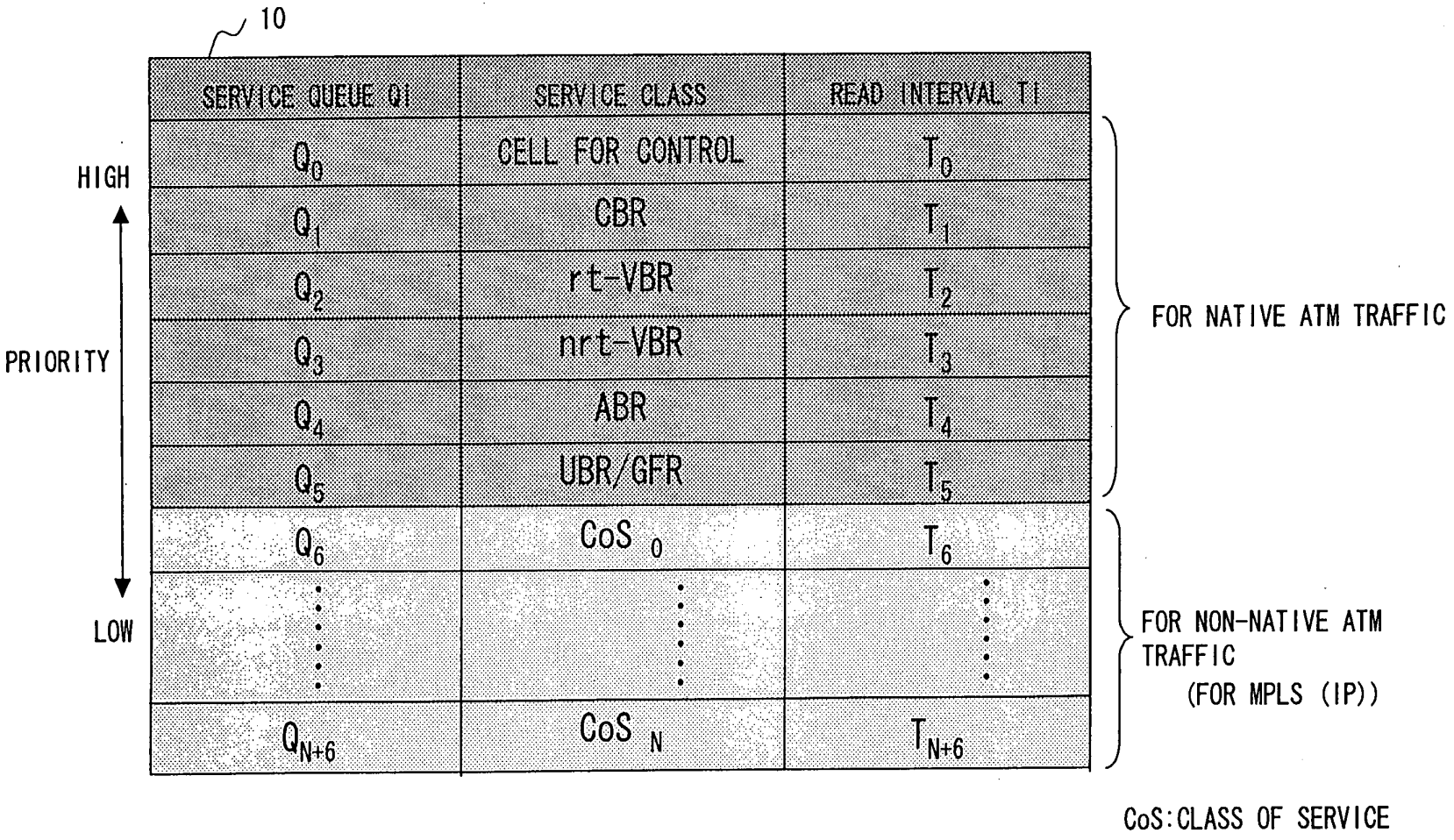

1 LINE INTERFACE
2
3 INPUT CELL PROCESSOR
6
SCHEDULER
7
COUNTER CIRCUIT
4a
10
SERVICE QUEUE
WRITE CONTROLLER
8
9
CELL BUFFER AREA
INTERFACE
CALL PROCESSOR
LINE
LINE TERMINATING EQUIPMENT
SCHEDULER
COUNTER CIRCUIT
SERVICE QUEUE
WRITE CONTROLLER
CELL BUFFER AREA
SWITCH MATRIX
5 OUTPUT CELL PROCESSOR
4b

FIG. 2


10
SERVICE QUEUE Qi
SERVICE CLASS
READ INTERVAL Ti
HIGH
PRIORITY
LOW
Q_0
CELL FOR CONTROL
T_0
Q_1
CBR
T_1
Q_2
rt-VBR
T_2
Q_3
nrt-VBR
T_3
Q_4
ABR
T_4
Q_5
UBR/GFR
T_5
FOR NATIVE ATM TRAFFIC
Q_6
CoS_0
T_6
Q_{N+6}
CoS_N
T_{N+6}
FOR NON-NATIVE ATM TRAFFIC (FOR MPLS (IP))
CoS:CLASS OF SERVICE

FG66③

FIG. 3

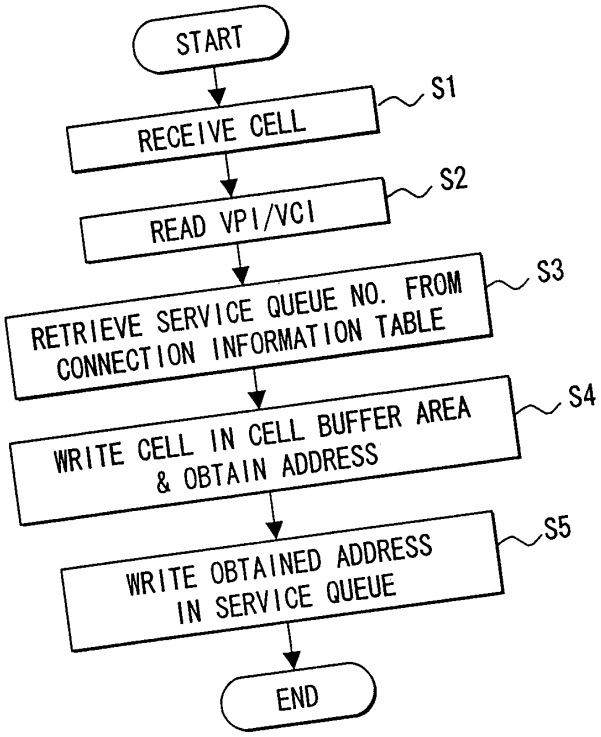
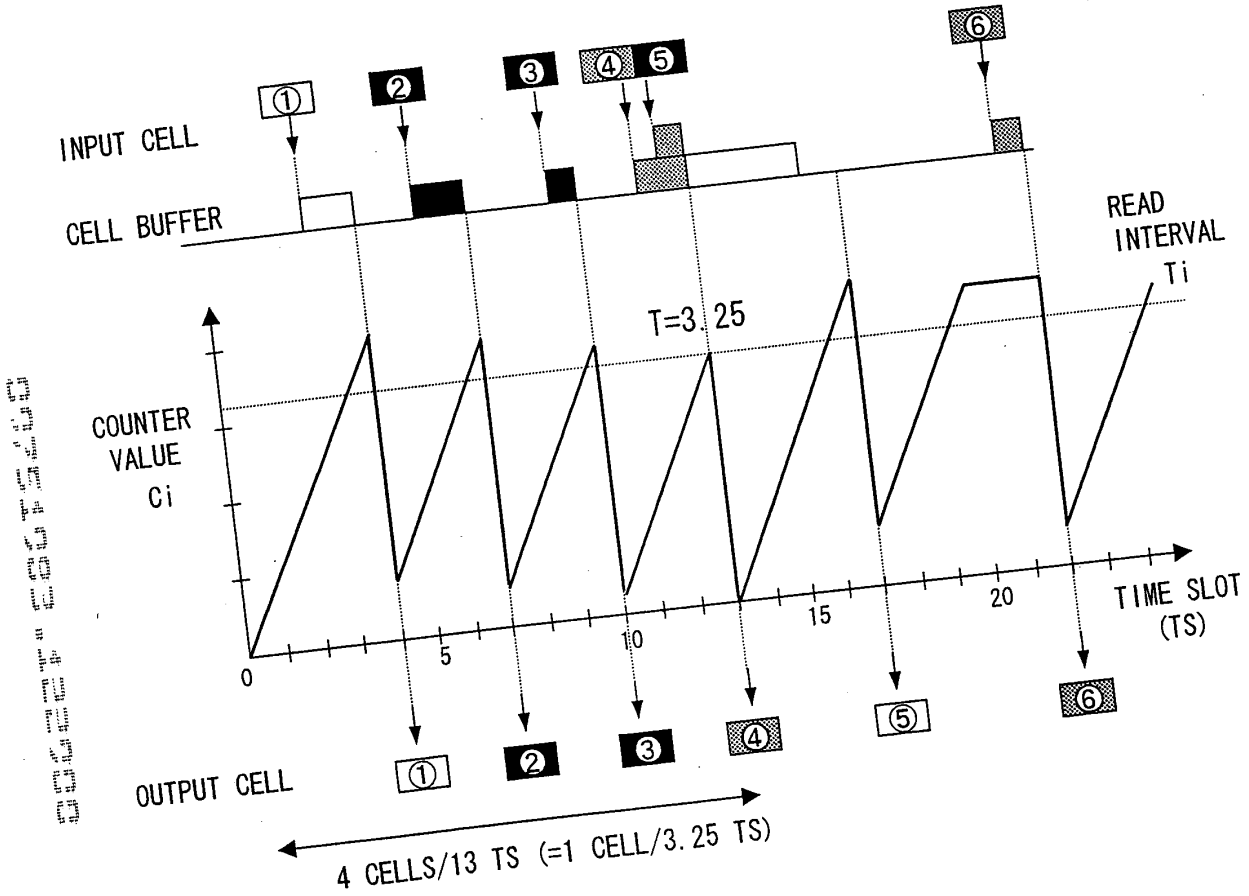


FIG. 4

ENTRY NO.	VPI	VCI	SERVICE QUEUE NO.
0	15	13	Q_4
1	21	19	Q_6
⋮	⋮	⋮	⋮

FG 66(4)

FIG. 5


INPUT CELL
CELL BUFFER
READ INTERVAL
Ti
T=3.25
COUNTER VALUE
Ci
0
5
10
15
20
TIME SLOT
(TS)
OUTPUT CELL
4 CELLS/13 TS (=1 CELL/3.25 TS)

FG 66(5)

FIG. 6

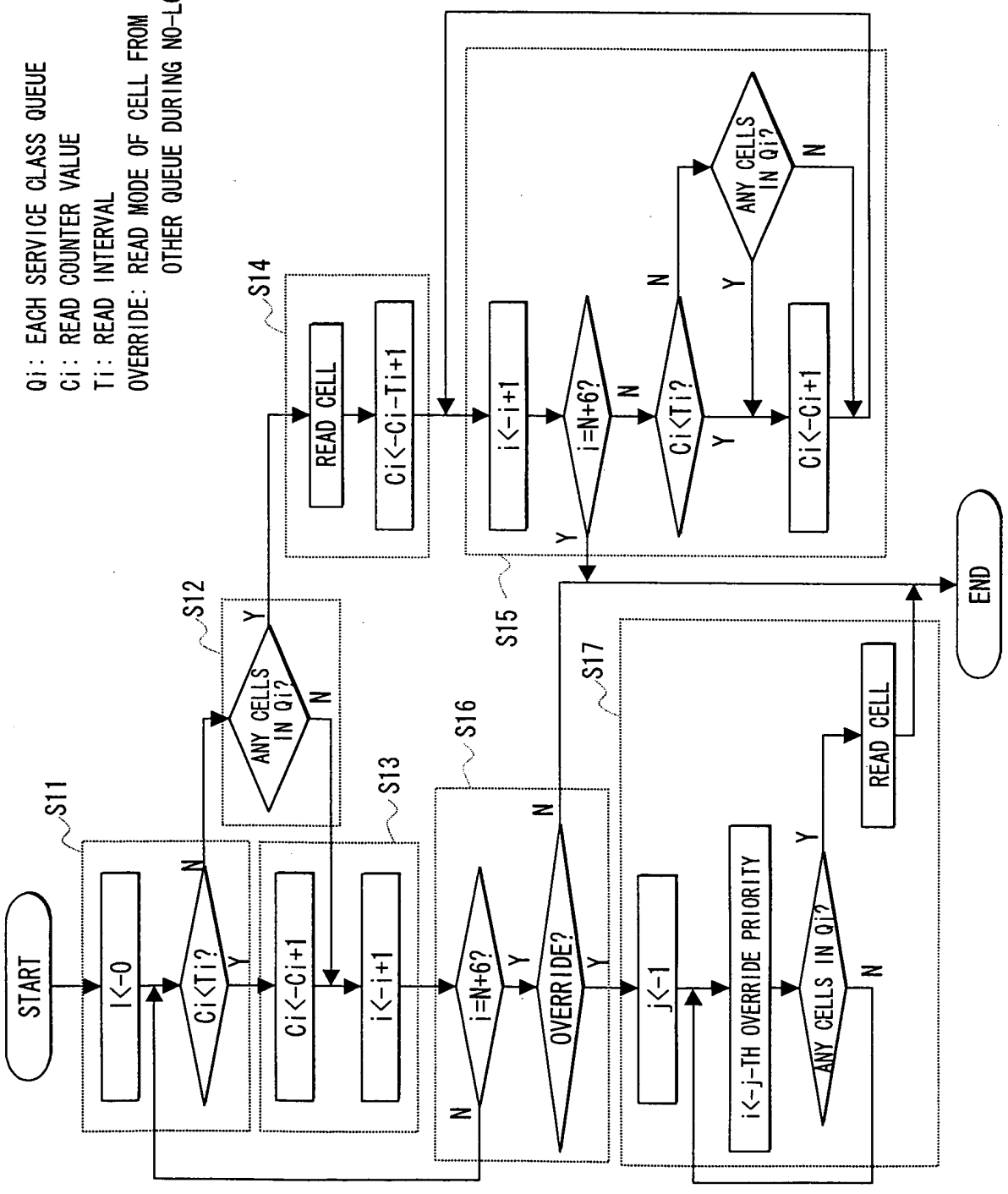
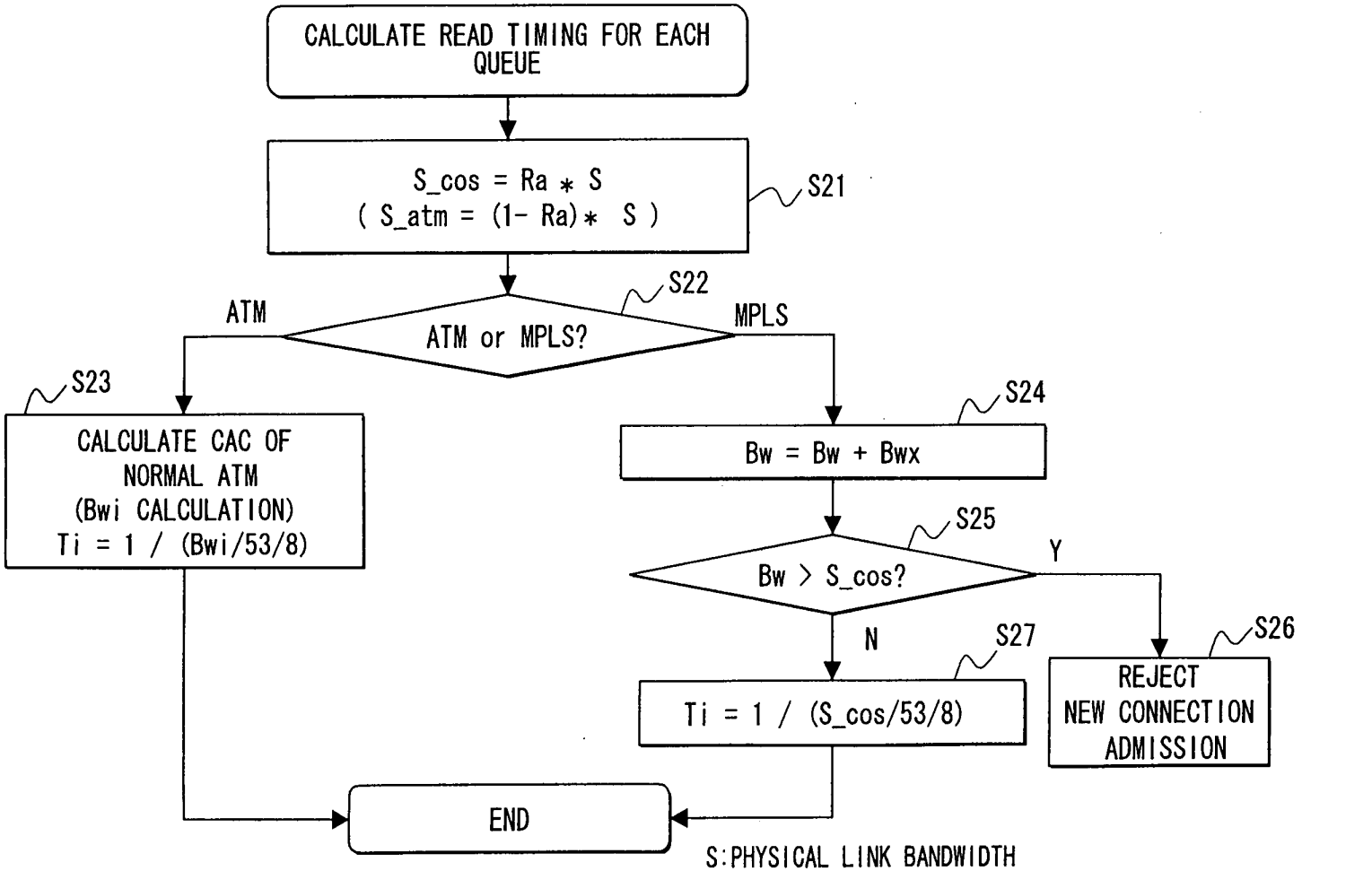

Qi: EACH SERVICE CLASS QUEUE
Ci: READ COUNTER VALUE
Ti: READ INTERVAL
OVERRIDE: READ MODE OF CELL FROM OTHER QUEUE DURING NO-LOAD
START
S11
I<-0
Ci<Ti?
Y
N
S12
ANY CELLS IN Qi?
Y
N
Ci<-Ci+1
S13
i<-i+1
S14
READ CELL
Ci<-Ci-Ti+1
S15
i<-i+1
i=N+6?
Y
N
Ci<Ti?
Y
N
ANY CELLS IN Qi?
Y
N
Ci<-Ci+1
S16
i=N+6?
Y
N
OVERRIDE?
Y
N
S17
j<-1
i<-j-TH OVERRIDE PRIORITY
ANY CELLS IN Qi?
Y
N
READ CELL
END

FIG. 7

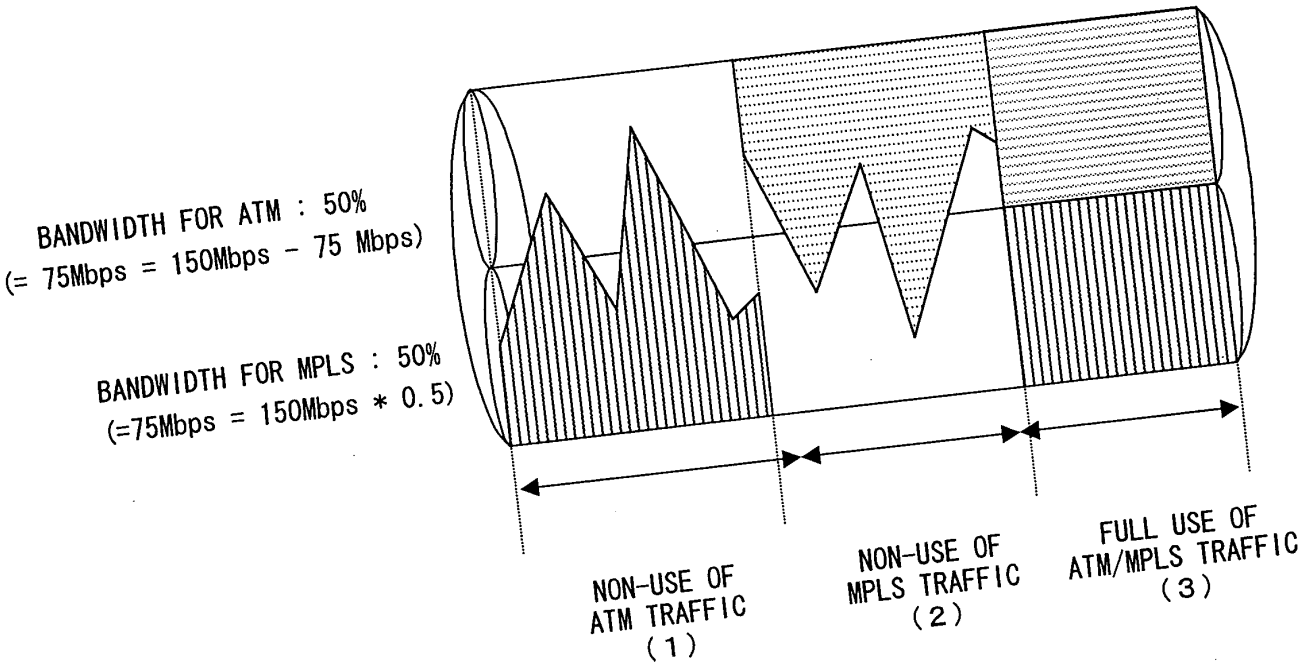


S:PHYSICAL LINK BANDWIDTH
Ra: BANDWIDTH ALLOCATION RATE FOR MPLS
S_cos: BANDWIDTH FOR MPLS
S_atm: BANDWIDTH FOR ATM SERVICE
Bwi: READ BANDWIDTH FROM EACH SERVICE QUEUE
Bw: BANDWIDTH DEMANDED BY EACH CONNECTION OF MPLS
Bwx: BANDWIDTH DEMANDED BY NEWLY ADMITTING CONNECTION

FG66(2)

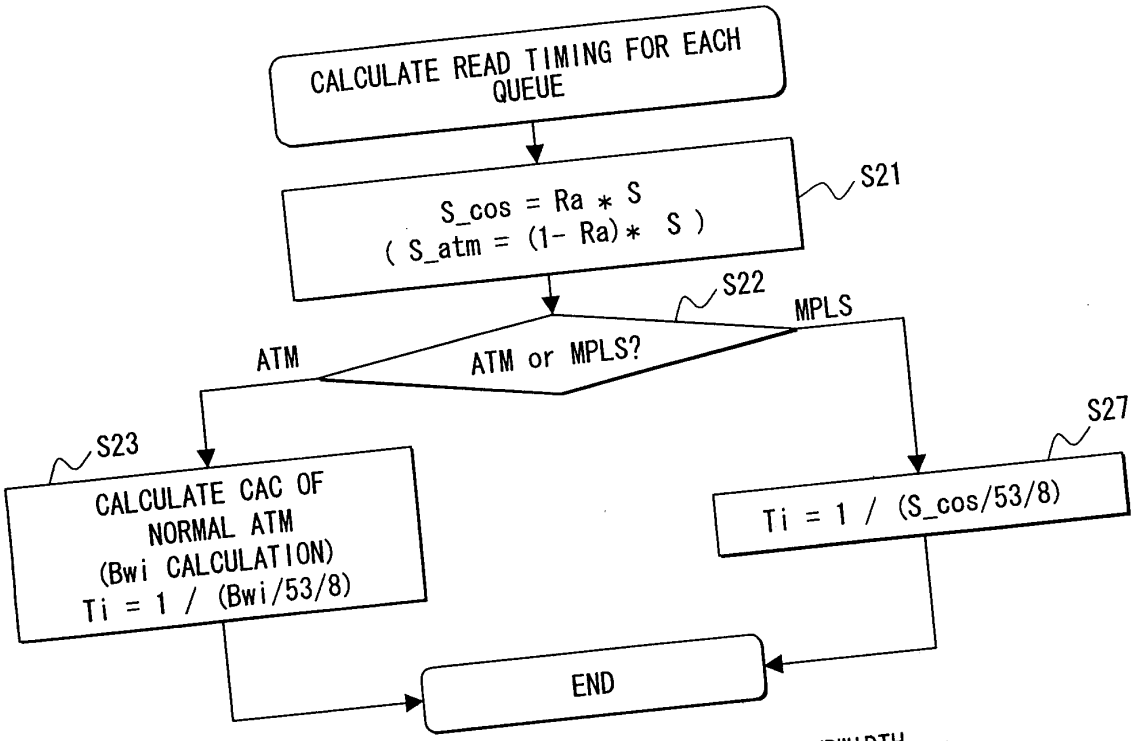
DOCSET-2007520

FIG. 8



09622[illegible]

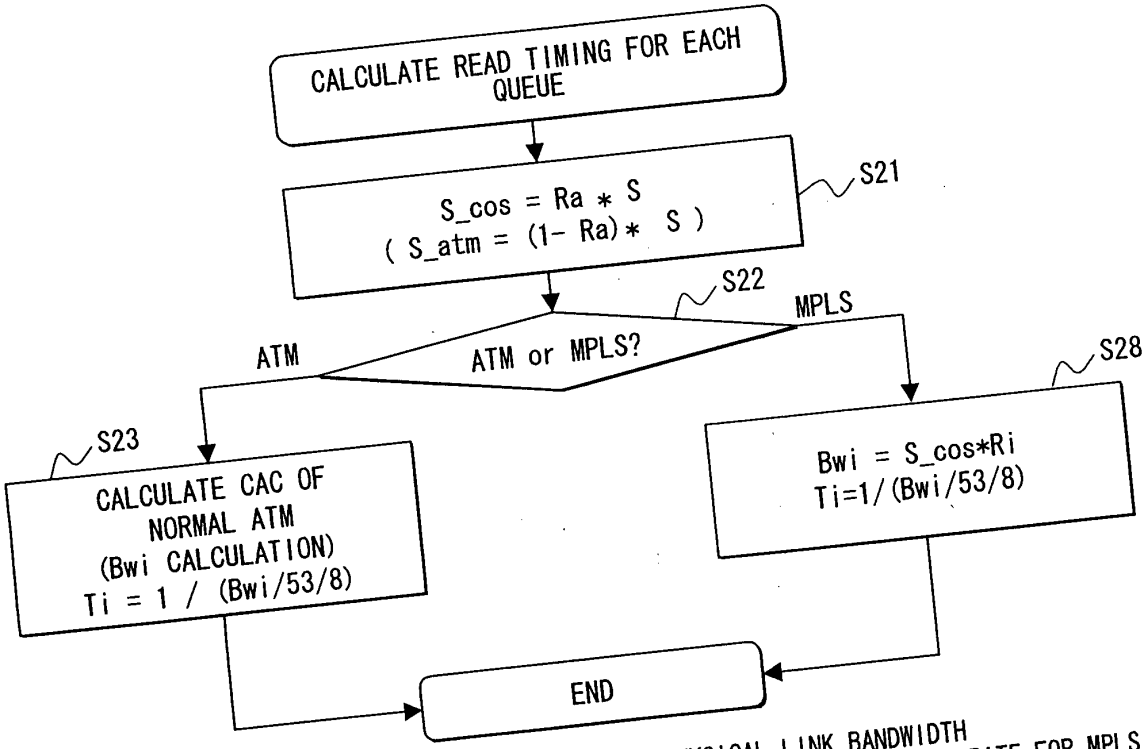
FIG. 9



S:PHYSICAL LINK BANDWIDTH
Ra: BANDWIDTH ALLOCATION RATE FOR MPLS
S_cos: BANDWIDTH FOR MPLS
S_atm: BANDWIDTH FOR ATM SERVICE
Bwi: READ BANDWIDTH FROM EACH SERVICE QUEUE
Bw: BANDWIDTH DEMANDED BY EACH CONNECTION OF MPLS
Bwx: BANDWIDTH DEMANDED BY NEWLY ADMITTING CONNECTION

FG 66 (9)

FIG. 10



S:PHYSICAL LINK BANDWIDTH
Ra: BANDWIDTH ALLOCATION RATE FOR MPLS
S_cos: BANDWIDTH FOR MPLS
S_atm: BANDWIDTH FOR ATM SERVICE
Bwi: READ BANDWIDTH FROM EACH SERVICE QUEUE
Ri: BANDWIDTH ALLOCATION RATE FOR PRIORITY i

FIG. 11

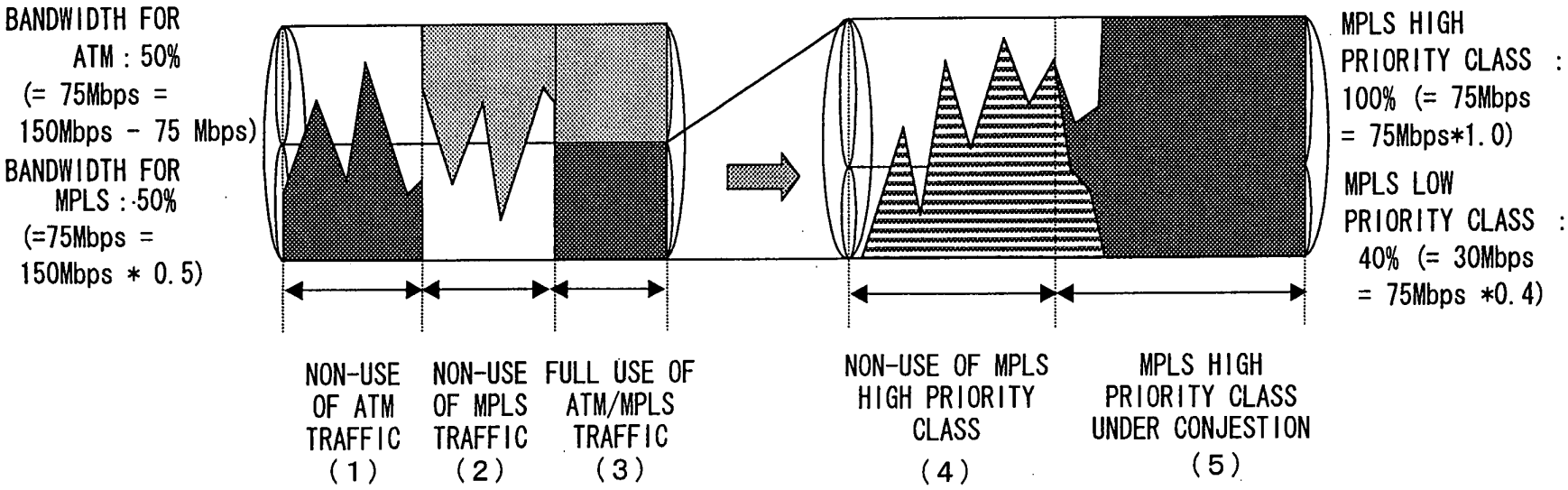

BANDWIDTH FOR ATM : 50% (= 75Mbps = 150Mbps - 75 Mbps)
BANDWIDTH FOR MPLS : 50% (=75Mbps = 150Mbps * 0.5)
MPLS HIGH PRIORITY CLASS : 100% (= 75Mbps = 75Mbps*1.0)
MPLS LOW PRIORITY CLASS : 40% (= 30Mbps = 75Mbps *0.4)
NON-USE OF ATM TRAFFIC (1)
NON-USE OF MPLS TRAFFIC (2)
FULL USE OF ATM/MPLS TRAFFIC (3)
NON-USE OF MPLS HIGH PRIORITY CLASS (4)
MPLS HIGH PRIORITY CLASS UNDER CONJESTION (5)

FIG. 12

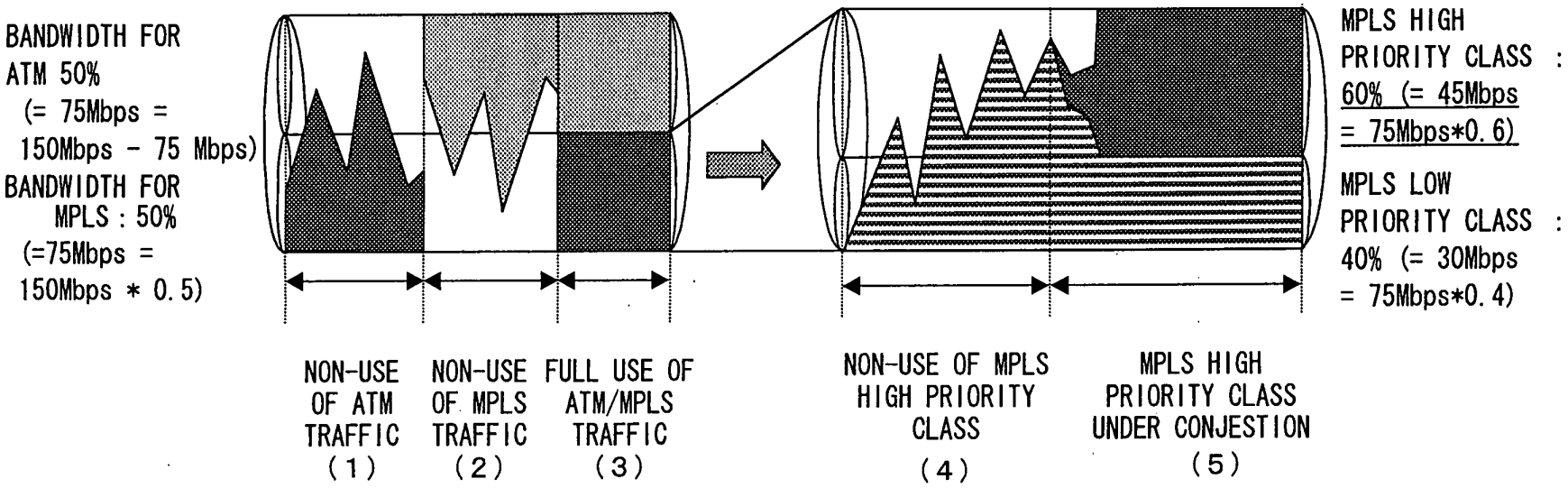
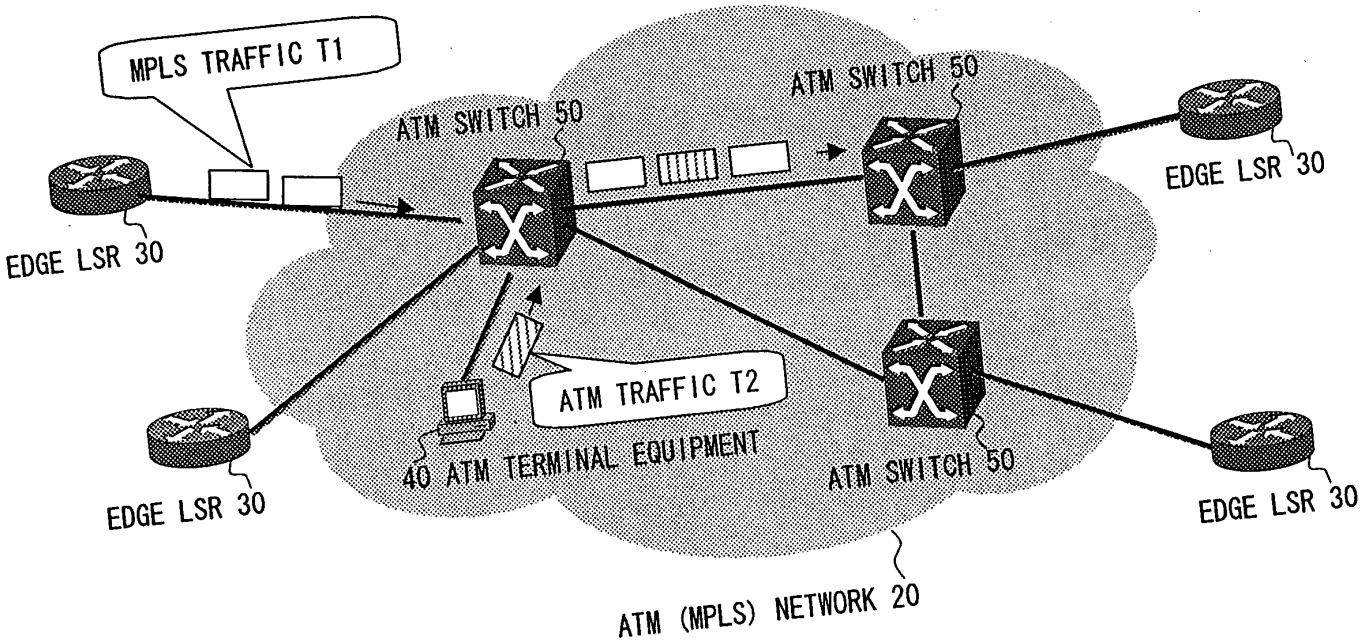

BANDWIDTH FOR ATM 50% (= 75Mbps = 150Mbps - 75 Mbps)
BANDWIDTH FOR MPLS : 50% (=75Mbps = 150Mbps * 0.5)
MPLS HIGH PRIORITY CLASS : 60% (= 45Mbps = 75Mbps*0.6)
MPLS LOW PRIORITY CLASS : 40% (= 30Mbps = 75Mbps*0.4)
NON-USE OF ATM TRAFFIC (1)
NON-USE OF MPLS TRAFFIC (2)
FULL USE OF ATM/MPLS TRAFFIC (3)
NON-USE OF MPLS HIGH PRIORITY CLASS (4)
MPLS HIGH PRIORITY CLASS UNDER CONJESTION (5)

FIG. 13



LSR: LABEL SWITCHING ROUTER

FIG. 14

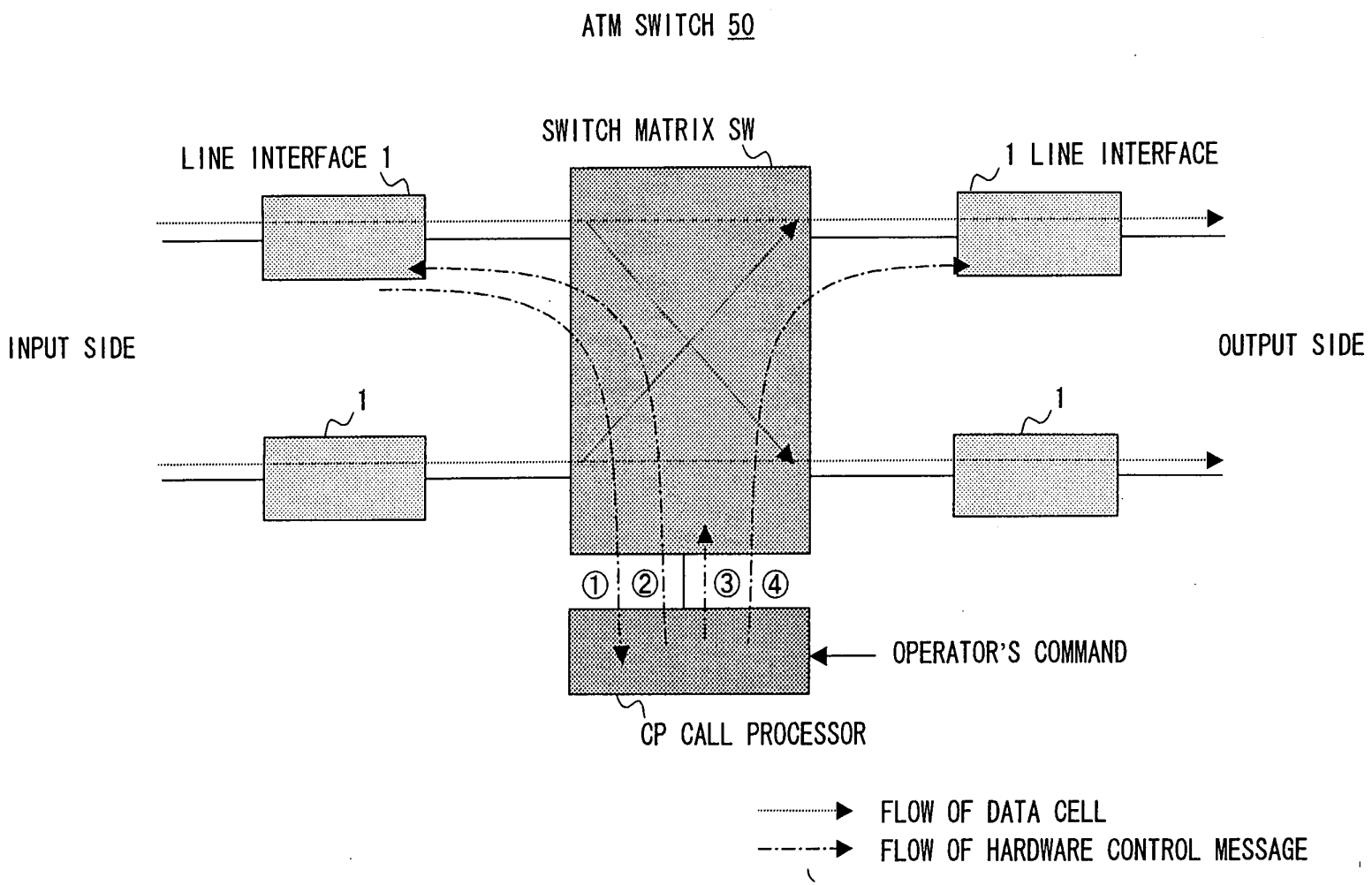
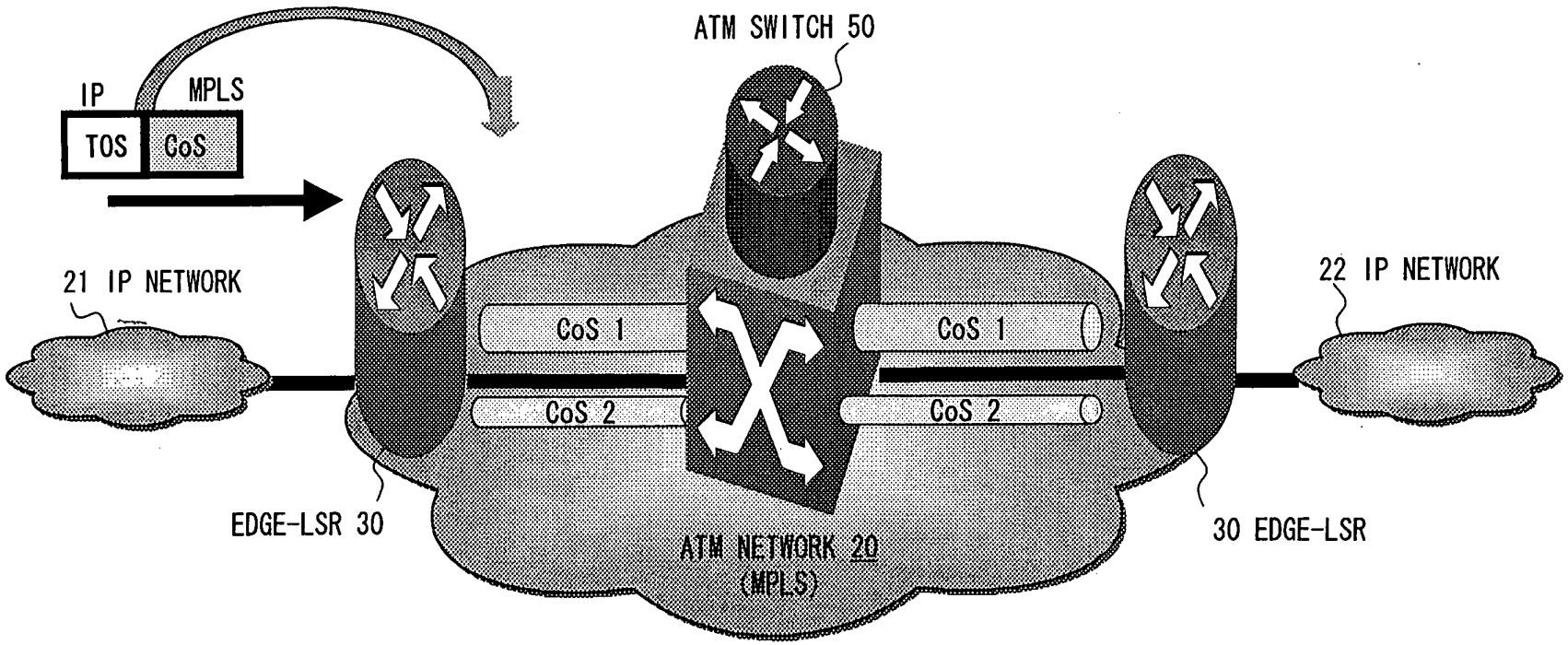

ATM SWITCH 50
SWITCH MATRIX SW
LINE INTERFACE 1
1 LINE INTERFACE
INPUT SIDE
OUTPUT SIDE
1
1
① ② ③ ④
OPERATOR'S COMMAND
CP CALL PROCESSOR
FLOW OF DATA CELL
FLOW OF HARDWARE CONTROL MESSAGE

FIG. 15


ATM SWITCH 50
IP
MPLS
TOS
CoS
21 IP NETWORK
22 IP NETWORK
CoS 1
CoS 2
CoS 1
CoS 2
EDGE-LSR 30
30 EDGE-LSR
ATM NETWORK 20
(MPLS)